Cylindrical Field Effect Transistor: A Full Volume Inversion Device

Thesis by

HOSSAIN MOHAMMED FAHAD

In Partial Fulfillment of the Requirements

for the degree of

Masters of Science

King Abdullah University of Science and Technology, Thuwal,
Kingdom of Saudi Arabia
December, 2010

Defended (December 11, 2010)

SIGNATURE APPROVALS FORM

The thesis of Hossain Mohammed Fahad is approved.

KHALED SALAMA	Khaled Salama	Dec 13th 2010
Committee Member Name	Signature	Date
Husam Alshareef		Dec 13th, 2010
Committee Member Name	Signature	Date
Muhammad Mustafa Hassan		14th DEC 2010
Name, Committee Chair	Signature	Date

Abstract

The increasing demand for high performance as well as low standby power devices has been the main reason for the aggressive scaling of conventional CMOS transistors. Current devices are at the 32nm technology node. However, due to physical limitations as well as increase in short-channel effects, leakage, power dissipation, this scaling trend cannot continue and will eventually hit a barrier. In order to overcome this, alternate device topologies have to be considered altogether. Extensive research on ultra thin body double gate FETs and gate all around nanowire FETs has shown a lot of promise. Under strong inversion, these devices have demonstrated increased performance over their bulk counterparts. This is mainly attributed to full carrier inversion in the body. However, these devices are still limited by lithographic and processing challenges making them unsuitable for commercial production. This thesis explores a unique device structure called the CFET (Cylindrical Field Effect Transistors) which also like the above, relies on complete inversion of carriers in the body/bulk. Using dual gates; an outer and an inner gate, full-volume inversion is possible with benefits such as enhanced drive currents, high I_{on}/I_{off} ratios and reduced short channel effects.

Acknowledgements

All praise is to Allah the almighty.

I would like to express my deepest gratitude towards my supervisor and mentor Dr. Muhammad Hussain for the constant motivation, never ending support and guidance. I am also heartily thankful to Dr. Casey Smith for his invaluable advice and support throughout the course of this project. This work would not have been possible without their guidance. I would also like to extend a special thank you to Dr. Khaled Salama and Dr. Husam AlShareef for taking out the time to review this thesis. Finally, I am grateful to my parents, my siblings and friends for their moral support.

Table of Contents

List of Abbreviations

FET	Field Effect Transistor
NMOS	n-channel Metal Oxide Semiconductor Field Effect Transistor
CFET	Cylindrical Field Effect Transistor
GAA	Gate All Around
SOI	Silicon On Insulator
DGFET	Double Gate Field Effect Transistor
UTB	Ultra Thin Body
NWFET	Nanowire Field Effect Transistor
OGAA	Outer Gate All Around – *CFET outer gate*
CSG	Core Shell Gate – *CFET inner gate*
S/D	Source/Drain
TCAD	Technology Computer-Aided Design
SS	Sub-Threshold Slope
DIBL	Drain Induced Barrier Lowering
TiN	Titanium Nitride

List of Figures

Introduction

Since its inception in 1954, the silicon based transistor has been the single key player in nearly all technological achievements to date. Applications spanning consumer products, medicine all the way to space exploration has been a catalyst for the progressive reduction of transistor dimensions. In keeping up with the technology roadmap (ITRS) [1], advances in lithographic and processing technologies has reduced the feature size of conventional CMOS devices so much that a few years from now it will become physically impossible to continue Moore`s Law. Problems such as increased heat dissipation, short channel effects (SCE), leakage current plague conventional devices which are currently at the 32 nm technology node. To go beyond this, it is imperative to focus on alternate device topologies and engineer new materials. The ultimate goal then is to establish a new baseline for unconventional devices and to continue the scaling trend.

The problem of short channel effects in planar MOS devices has been known since late 1970. It was realized that decreasing device gate lengths would cause the source and drain depletion regions to interact with each other, leading to reduction of threshold voltage (SCE) and increased off-state leakage current. At the time, to mitigate this problem, the widths of the depletion regions were reduced by increasing the bulk/body doping. However, early experimental results quickly pointed out that increased body doping led to degraded sub-threshold swing, carrier mobility, random dopant fluctations and increased device capacitances. All of these are against device scaling and were instrumental in the pushing the focus on multiple gate MOS devices.

The idea of multiple gate devices evolved from the development of the double gate MOSFET (DGFET). In 1987, Balestra et al., successfully demonstrated the advantages to a DGFET. Introducing a back gate below the buried oxide (BOX) in a single gate silicon on insulator (SOI) FET with an ultra thin body, gave better device control in terms of gate electrostatics. Basically, the second gate helps shield the channel from penetrating drain electric field lines. Balestra`s results indicated increased output drive current, low sub-threshold slope and higher trans-conductance as opposed to the single gate FET [2]. They attributed all of this to volume inversion of minority carriers in the DGFET body. Volume inversion is discussed in detail in chapter 2. With the DGFET, the body no longer required heavy doping and so proved itself to be a viable candidate for future CMOS technology. However, gate alignment issues and problems associated with ultra thin bodies are still a major drawback of the DGFET.

The development of the DGFET set the wheel in motion and within a couple of years the first three dimensional tri-gate device was developed. In 1989, Hisamoto et al., fabricated the fully-depleted lean channel transistor, DELTA. Here, a bulk ultrathin SOI crystal grown vertically by selective oxidation was used for the body of the device. A low sub-threshold slope of 62 mV/dec and an output drive current of 0.45 mA was obtained at a drain voltage of 3.5V. The device had an effective gate length of 0.57 um. This was considered a very early version of the modern FinFET [3]. It was also the first device to utilize elevated source and drain regions (elevated S/D). However, since planar MOSFETs were meeting the needs of the industry at the time, DELTA did not gain popularity.

In 2000, the industry realized that the physical barrier (as predicted by the ITRS) was closing in on planar CMOS devices. This helped revive the DELTA but this time in the form of the FinFET. Hisamoto et al. demonstrated the first n-channel FinFET having a gate length of 17 nm. A thin silicon fin 10 nm thick serves as the body of the FET [4]. This device exhibited very good sub-threshold swing and reduced short channel effects. Hisamoto also showed that by increasing the number of silicon fins, the current drivability could be increased proportionally. In addition to this, FinFET fabrication is compatible with conventional CMOS process technologies. There are two variants of the FinFET, the Ω-gate and the Π-gate. Recent work by several groups has confirmed its enhanced performance making it a very popular choice for beyond 2010 electonics. However, there are still certain problems that are delaying the transistion of FinFETs from the research phase to commercialization. Some of them include non uniformity of the fins, BiCMOS integration, S/D series parasitics, degraded mobility. Some of these have already been addressed. In 2005, metal gates and high-K dielectrics were first incorporated in the gate stack of planar MOSFETs. In addition to this, strain engineering for enhanced mobility has pushed the limits of bulk MOSFETs, squeezing out a few more years from them. Because of this there was no immediate urgency in getting the FinFET commercialized.

In the pursuit for the ultimate device for applications in high-performance (HP) or low-standby power (LSTP) regime, multiple gate devices have once more evolved; this time from the FinFET technology. Gate all around nanowire FETs (GAA NWFET) have recently taken the spotlight by exhibiting excellent gate electrostatic control. Several groups have demonstrated GAA NWFETs with very high Ion/Ioff ratio, low sub-

threshold swing, and suppressed short channel effects [5-9]. However, commercialization of GAA NWFETs is a challenge as their fabrication is incompatible with current CMOS process technologies. A nanowire (NW) is used as the body for these devices. So, the critical fabrication stage is in the NW growth and assembly/alignment. There are several techniques for NW growth. Most commonly they are grown using the vapor-liquid-solid (VLS) technique. This technique produces a forest of NWs rather than an ordered array. Due to the lack of controlled growth, it becomes a challenge during handling and alignment to fabricate a NWFET. Of course there have been several laboratory demonstrations of NWFETs utilizing template based growth, Super Lattice Nano Pattering (SNAP), self-limiting oxidation [7][10]. Although a lot of focus has been put on homogenous silicon based NWFETs, there has been a rising interest in III-V NWFETs. This is mainly due to the excellent carrier transport properties provided by these materials. Wang et al. demonstrated a pMOS Germanium NWFET having a hole mobility of almost 600 cm^2/Vs [24]. Zhang et al. showed that gate all around Germanium NWFET had improved performance and better electrostatic control over previously reported NWFETs [25]. Recent studies have indicated electron mobilities of ~ 3000 cm2/Vs in InAs NWFETs [26]. Besides these, experimental studies have indicated the capability of heterostructure NWFETs (such as the Ge/Si Core/Shell nanowires) for high-performance FETs [27]. However, all these are still laboratory demonstrations. Although there are assembly techniques for producing somewhat aligned arrays of nanowires, integration is still a challenge for NWFETs. So it is imperative to look for other alternative device topologies besides the ones described above.

This thesis proposes a new device topology called the cylindrical field effect transistor (CFET) that relies on full volume inversion of minority carriers for operation. 3D TCAD simulations are carried out on an n-channel CFET to assess its performance. The device architecture and simulation details are discussed in chapter 1. In Chapter 2, simulation results are presented. Volume inversion and its impact on SS, DIBL, SCE are discussed in moderate detail. In addition to this, comparison of performance is made between a simulated planar NMOS, GAA NWFET and the n-channel CFET. The proposed process flow for fabricating the CFET is described in chapter 3. This thesis concludes with a summary and future research objectives.

Chapter 1: CFET Device Architecture and Simulation Tool

The proposed structure of the cylindrical field effect transistor is depicted in Fig. 1.1. An n++ doped region serves as the source region. The n-channel CFET has got two gates. An outer GAA type gate (OGAA) and an inner core shell gate (CSG). Both the outer gate and the inner gate consists of a poly/metal/HK/oxide stack.

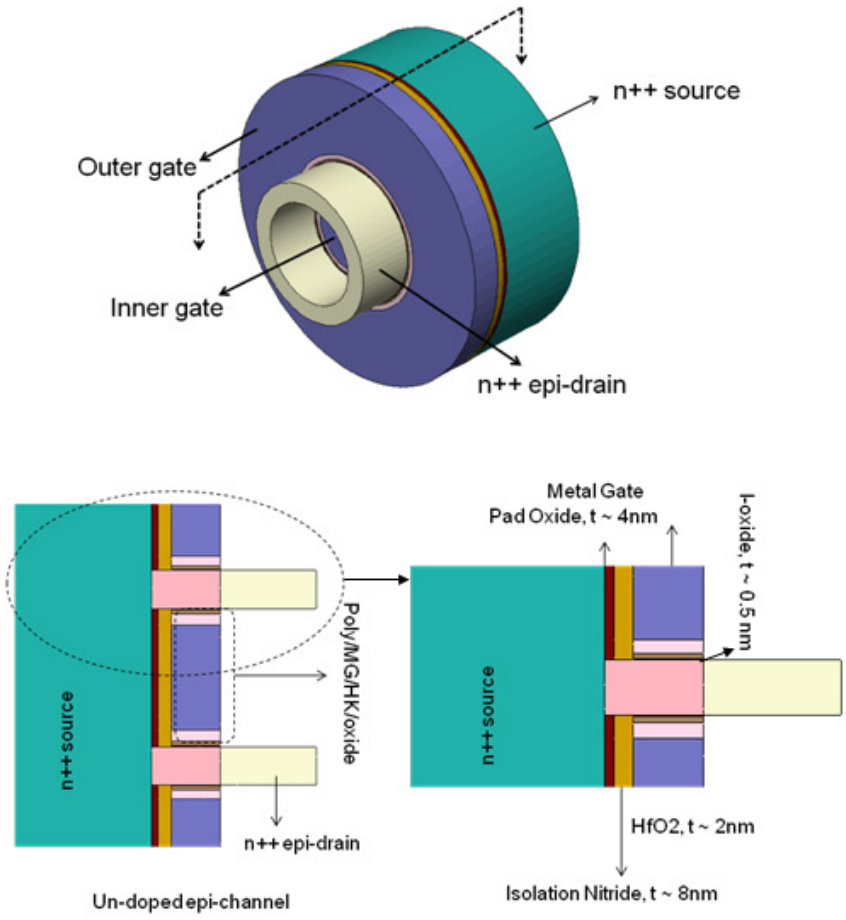

Fig. 1.1 Cylindrical Field Effect Transistor (CFET): Top(3D-model), Bottom (2D-cross section along dotted line)

The metal gate used for the simulation is a mid-band gap material. Un-doped epitaxial silicon is grown from the openings to n++ source, till it just mushrooms over the gate stack. The portion of the epitaxial silicon along the gate stack forms the channel/body of the device. The portion of the epitaxial silicon just above the gate stack is n++ doped to form the drain. Detailed process steps for the CFET are covered in chapter 3. The simulated device has a gate length of 30 nm and body (ring) width of 20 nm. The source and the drain are doped with arsenic at a constant doping level of 10^{20} cm^{-3} compliant with the ITRS. However such an ideal doping profile is physically impossible as there will always be small amounts of dopant shifts between regions during activation annealing.

Sentaurus TCAD has been used to simulate the CFET architecture (Fig. 1.1) at the device level. Because the CFET is a short channel device (Lg = 30 nm and Wsi = 20nm), long channel carrier transport models cannot be applied due to reasons discussed in chapter 2. Such reduced dimensions and the use of double gates (inner CSG and OGAA), increase quantum confinement effects in the CFET. Sentaurus provides built-in transport and quantization models for just this purpose; Hydrodynamic and Density-gradient models.

Hydrodynamic Transport Model

As mentioned above, the commonly used long channel drift diffusion model for carrier transport cannot be applied to the short channel CFET. This is because impact ionization rates and short channel effects such as velocity overshoot cannot be described using the long channel model. Usually to describe short channel transport, Monte-Carlo simulations are carried out to obtain solution of the Boltzman`s kinetic equation.

However, as this is a chance based approach, it requires extensive computation. Sentaurus`s built in hydrodynamic transport is based on an energy balance model and is a simpler form of the model described by Stratton and Bloteckjaer [11]. This model is a good comprise between computation time and accuracy. It serves the purpose on initial performance estimates of the CFET. The model assumes that the lattice temperature (T) and carrier temperatures (T_n and T_p) are unequal. The overall model consists of solving the Poisson and current continuity equations as well as energy conservation equation for the carriers and the lattice. The electron and hole current densities in this model are given by [12]:

$$\underset{J_n}{\rightarrow} = q\mu_n(n\nabla E_C + kT_n\nabla n + f_n^{td}kn\nabla T_n - 1.5nkT_n\nabla \ln m_n)$$

$$\underset{J_p}{\rightarrow} = q\mu_p(p\nabla E_V - kT_p\nabla p - f_p^{td}kp\nabla T_p - 1.5pkT_p\nabla \ln m_p)$$

In the above equations, the first term takes into consideration the contribution from spatial variations of electrostatic potential, electron affinity and the band gap. The three remaining terms combine the contributions from gradient of concentrations, carrier temperature gradients and spatial variation of the carrier effective mass (given as m_n and m_p) [12].

Density-Gradient Quantization Model

Because the CFET is a short channel device, quantization effects become important as the carrier wavelengths now become comparable to device dimensions. One of the most important quantization effect is the threshold voltage roll off with gate length reduction. This is a short channel effect (SCE) which was briefly discussed in the introduction and will be described again in chapter 2. There are several quantization models provided by Sentaurus TCAD. However, for the 3D short channel CFET, the Density-Gradient Quantization model was chosen. This numerically robust model can describe quantization effects in 2D and 3D structures, but is computationally slow compared to other available models (which cannot be used for 3D). It also describes the carrier distributions and terminal characteristics in short channel MOSFETs, SOI double gate structures and quantum wells with reasonable accuracy [12].

The CFET is proposed to have an un-doped pristine silicon channel. So coulomb scattering due to carrier-carrier interaction and carrier-dopant interaction is negligible. Also, as will be discussed in chapter 2, scattering due to interface and HK dielectrics is also negligible. However, in the simulation, due to the lack of an epi-Si material file, un-doped bulk silicon is used for the CFET channel. So in hopes of obtaining a results with higher accuracy, carrier mobility models incorporating coloumbic and interface scattering as well as high - K degradation is included in the simulation.

To see where the CFET performance metrics stand, the results from the CFET simulations are compared with those of a simulated short-channel planar NMOS as well . In addition to this, a GAA NWFET is also simulated. The latter is simulated by removing the inner CSG in the CFET device. A 3D structure of the GAA NWFET as well as a

cross section of the device is given in Fig. 1.2. In terms of device fabrication, the CFET is an extension of the GAA NWFET. This will be discussed in chapter 3.

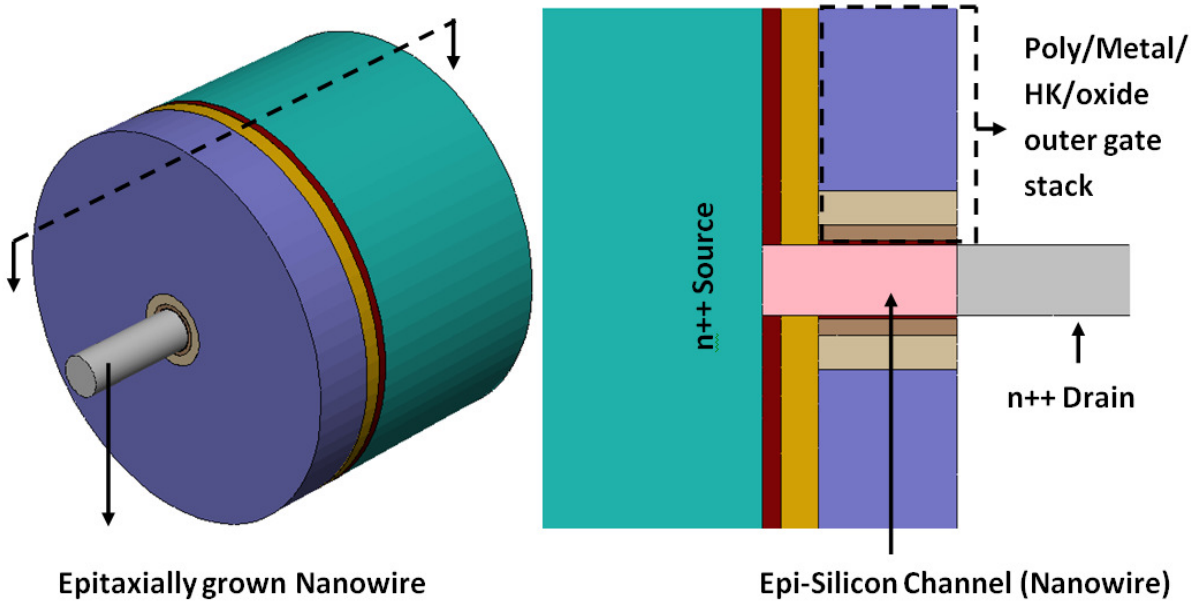

Fig. 1.2 Gate-all-around Nanowire FET (GAA-NWFET): Left (3D-model), Right (2D-cross section along dotted line)

Chapter 2: Volume Inversion and CFET Performance

As discussed in the introduction, enhanced device performance through volume inversion of minority carriers was first demonstrated by Balestra et al. using a SOI DGFET [2]. In such a device, if the silicon film is made sufficiently thin enough, the two inversion layers merge together. This interaction of inversion layers at opposing oxide/silicon interfaces results in some very interesting properties as the entire thin film behaves as the channel. In a DGFET, for a sufficiently thin silicon body, the interaction of the opposite inversion layers results in the carrier concentration to peak at the center of the film. Besides this, volume inversion also enhances the mobility of the minority carriers in long channel double gate devices. For short channel devices, volume inversion increases the carrier velocity. All of these enhancements are because of the shift of the carrier concentration centroid towards the center of the body. Due to this scattering due to interface and surface roughness is greatly reduced. However, these scattering mechanisms are not negligible as shown by Gamiz et al., at least not for long channel devices [13].

For the simulated CFET (Lg = 30 nm, ring width = 20 nm), the Ion (I_{dSat}) was determined to be **2.026 mA/um**. Fig. 2.1 shows the $I_d - V_g$ and $I_d - V_d$ plots that were obtained for the simulated device. The subsequent section of this chapter will describe reasons for the simulated CFET`s relatively high output drive current.

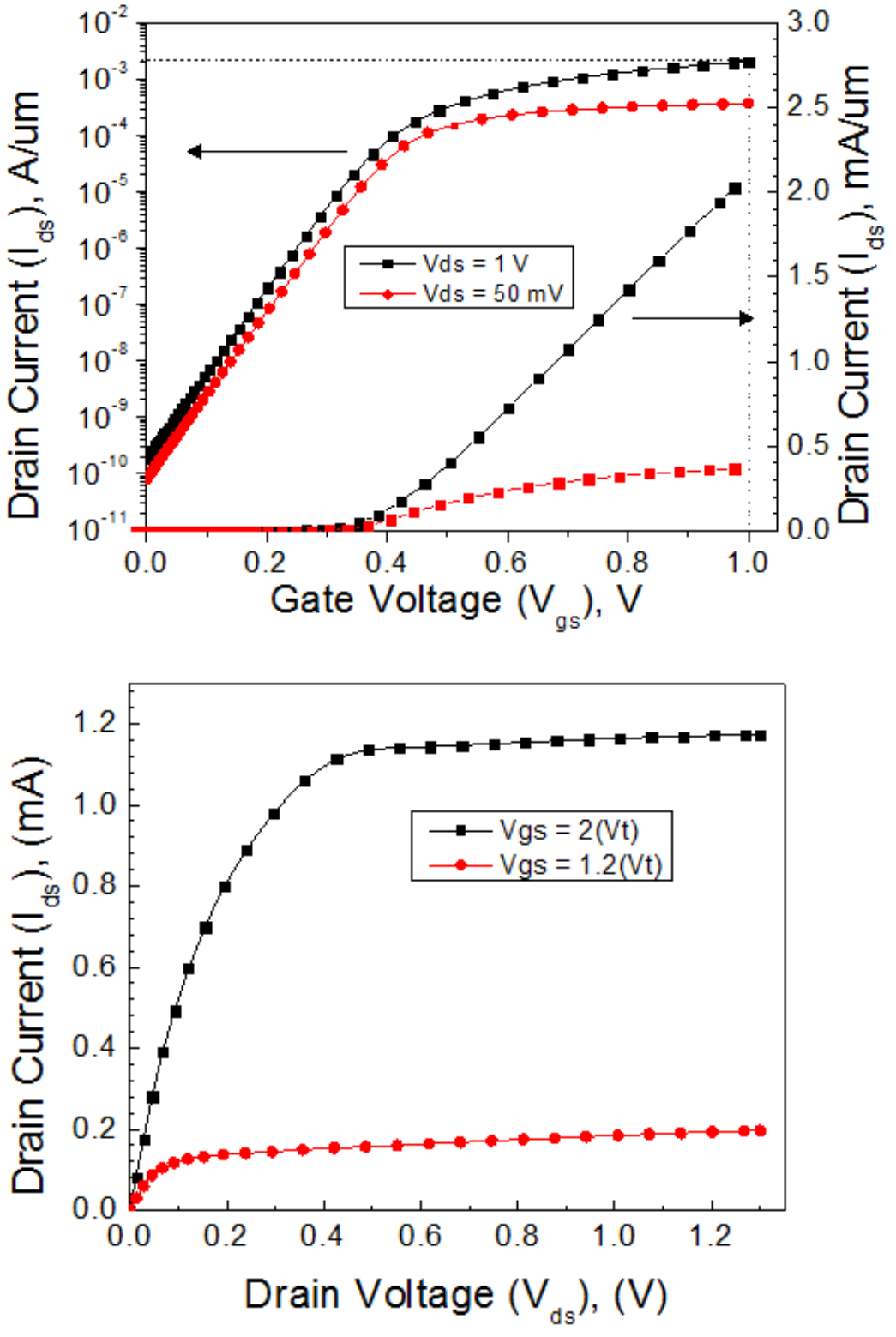

Fig. 2.1 Simulated CFET: (Top) Id-Vg plot (Bottom) Id - Vd plot.

Effect of Volume Inversion in CFET

Because of the use of double gates – the OGAA and the CSG; the CFET undergoes volume inversion just like in a DGFET. But unlike the DGFET, the unique architecture of the CFET does not require the silicon body to be extremely thin for full volume inversion. Fig. 2.2 depicts how the interaction of the two opposite inversion layers is affected by the width of the un-doped epitaxial silicon body. Full volume inversion increases the total number of carriers in the channel as shown in Fig. 2.3.

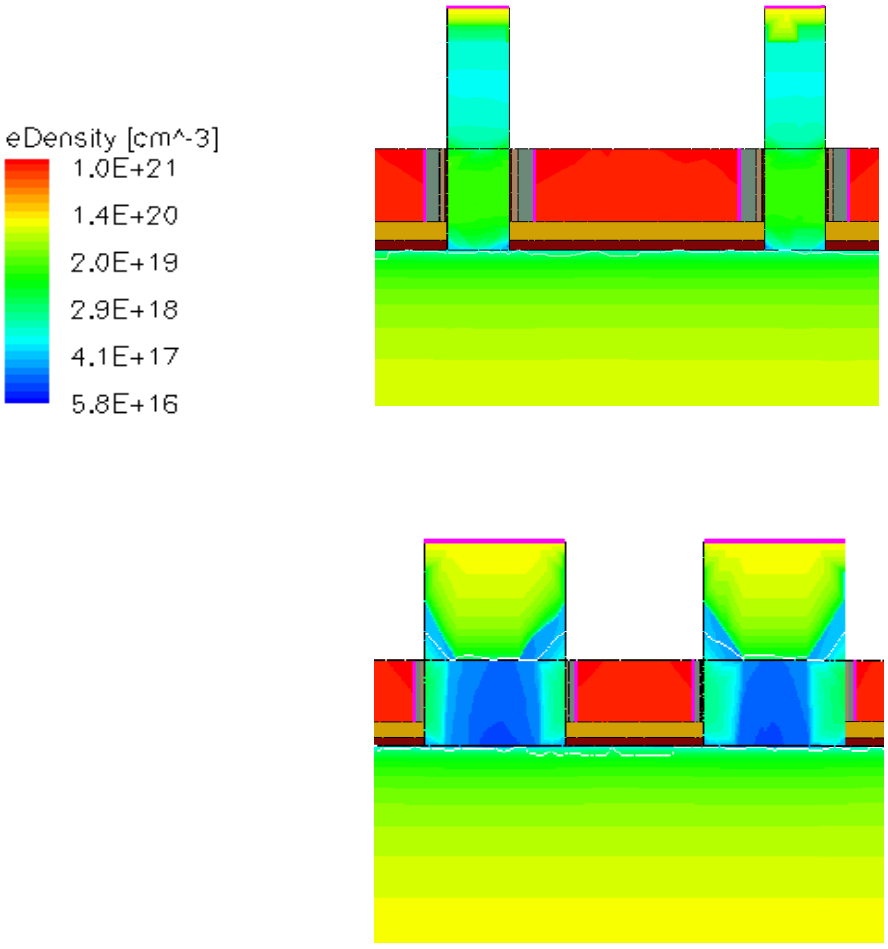

Fig. 2.2 Effect of varying CFET ring width on Volume Inversion: (Top) Channel Carrier Concentration at ring width of 20 nm (Bottom) Channel Carrier Concentration at ring width of 100 nm**.**

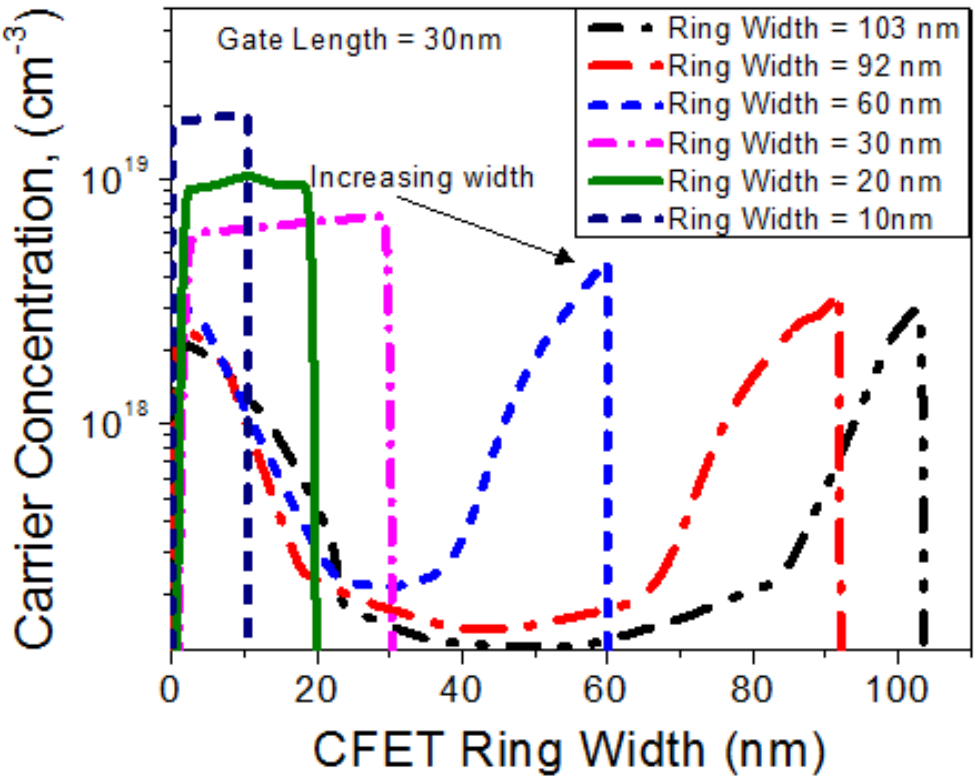

Fig. 2.3 Effect of CFET ring width variation on volume inversion.

Besides an enhanced carrier concentration, the CFET device has another unique advantage. From Fig. 2.3, it can be seen that the CFET is capable of volume inversion with thick bodies unlike SOI UTB DGFETs where the body thicknesses of 3-7 nm are required. Volume inversion is maintained up to CFET ring widths of 30 nm. Although it is not included in Fig. 2.3, volume inversion is maintained even at 40 nm body width.

Ballistic Carrier Transport

The CFET drain current can be described by the short channel model as follows [14]:

$$I_{dSat} = C_{ox} W v_{Sat} (V_{gs} - V_t)$$

This equation clearly shows that the drain current depends on the total inversion layer

charge (carrier concentration). The $C_{ox}(V_{gs} - V_t)$ term represents in the inversion layer charge.

The shape of the doping profile also has a unique effect on the drive current capability. The CFET is proposed to have an extremely abrupt dopant profile distribution across the source-channel-drain region as indicated in Fig. 2.4.

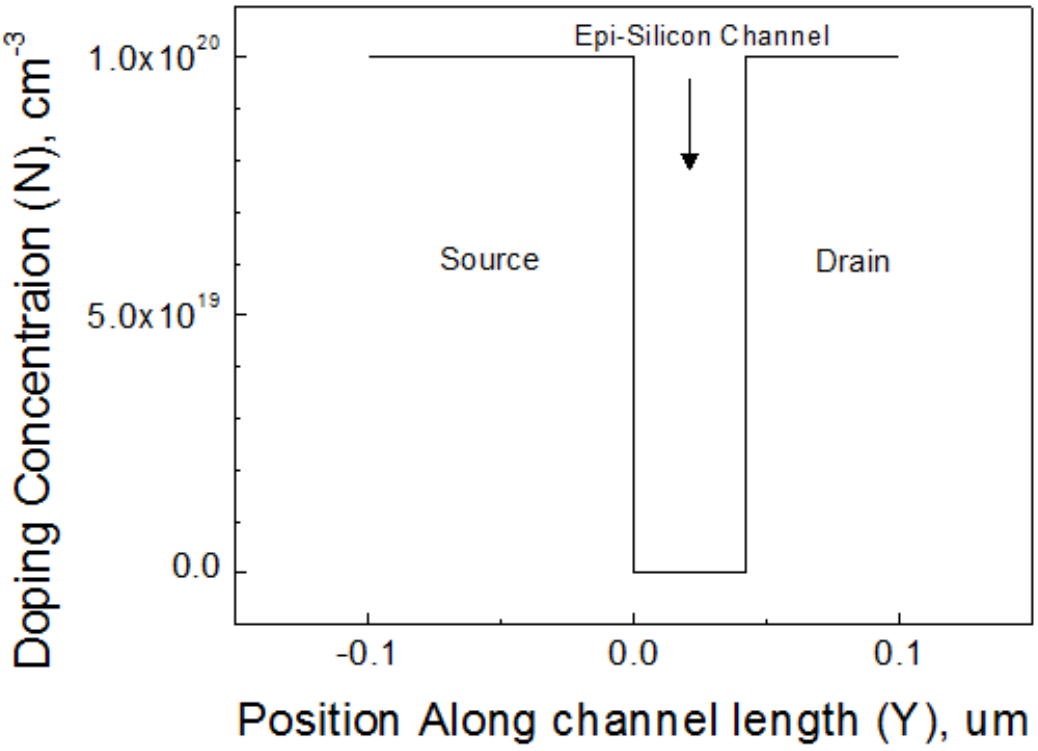

Fig. 2.4 Abrupt doping profile along source-channel-drain region

The commonly used drift-diffusion model for drive current used for the long channel device breaks down in the short channel case. In such devices, the relatively high output drain currents can be explained by the ballistic transport and scattering theory. According to this theory, under high drain bias, the on-current is set by the source-side thermal injection velocity of the carriers, v_T, given by [14]:

$$v_T = \frac{2h}{3\pi m_t}\sqrt{\frac{2C_{inv}(V_{gs} - V_t)}{\pi q}}$$

The thermal injection velocity is related to the device drive current by the following expression [14]:

$$I_{dSat} = C_{ox} W v_T (V_{gs} - V_t)$$

The proposed CFET can be classified as a short channel device. An abrupt profile results in a higher density-of-states (due to higher doping) in the source region near the electron barrier. Hence, carriers are injected with a very high velocity that approaches the ballistic limit [20]. This is a unique advantage of the CFET.

The simulated carrier velocity in the CFET channel is depicted in Fig. 2.5. In Fig. 2.6, a comparison of the CFET and planar NMOS carrier injection velocities confirm the near ballistic carrier velocities in the CFET. Besides the abrupt doping profile, ballistic transport in the CFET can also be attributed to negligible coulomb scattering in the un-doped epitaxially grown silicon channel. The lack of coulomb scattering also implies that the mobility of carriers does not have any effect on the output drain current.

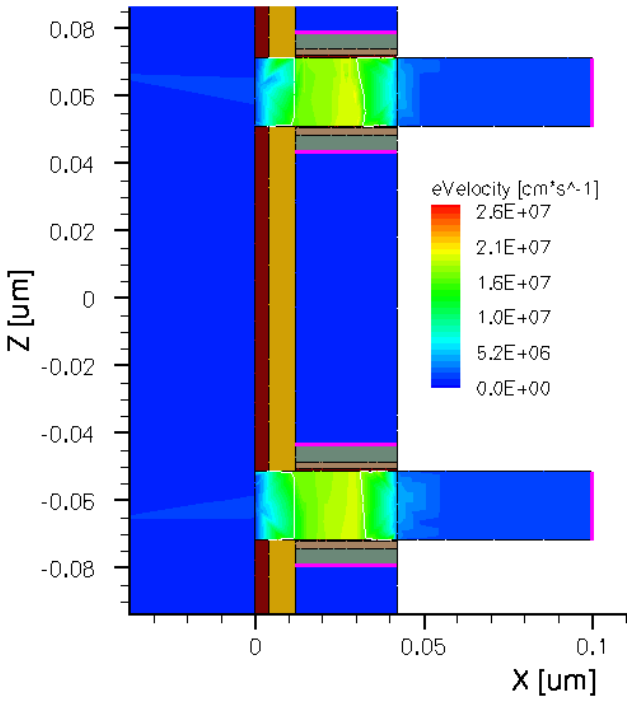

Fig. 2.5 Carrier velocity contour plot in simulated CFET (ring width = 20 nm, Lg = 30 nm)

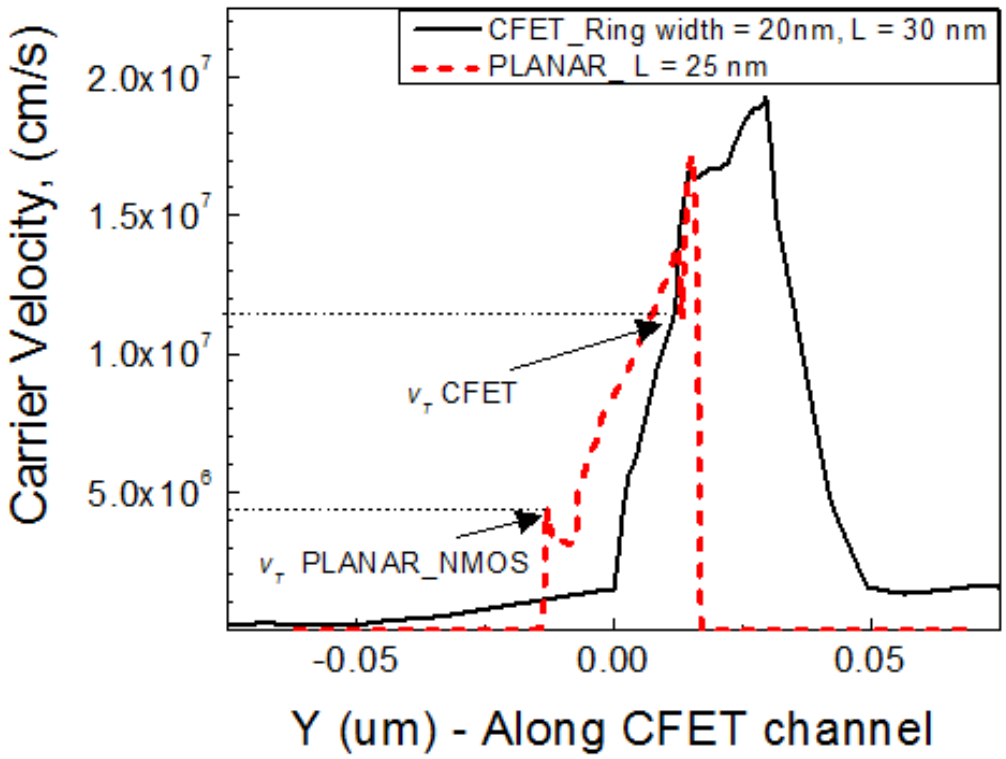

Fig. 2.6 Comparison of the carrier velocities in the channels of a planar NMOS and a CFET.

To summarize this section, TCAD simulations have shown that the CFET is capable of full volume inversion. Through this, the total number of electrons (carriers) in the inversion layer increases resulting in very high drive currents. It was also shown that near ballistic transportation occurs in the CFET due to high thermal injection velocities. This is made possible through the use of an extremely sharp doping profile in the source as well as the use of an un-doped epitaxially grown silicon layer as the channel material.

CFET Short Channel Effects and Performance Metrics

Normally, a measure of the device performance can be made from the ratio of the saturated (on-state) drive current (Id_{sat}) and off-state current (I_{off}). Simulation of the 30 nm gate length and 20 nm ring width CFET indicates an $\mathbf{I_{on}/I_{off}}$ ratio of $\mathbf{10^7}$. The scatter plot in Fig. 2.7 compares the simulated I_{on}/I_{off} ratio of the CFET, the GAA NWFET and a planar NMOS at different gate lengths. In addition to this, the plot also compares the I_{on}/I_{off} performance of some of the best reported NWFETs and conventional bulk FETs.

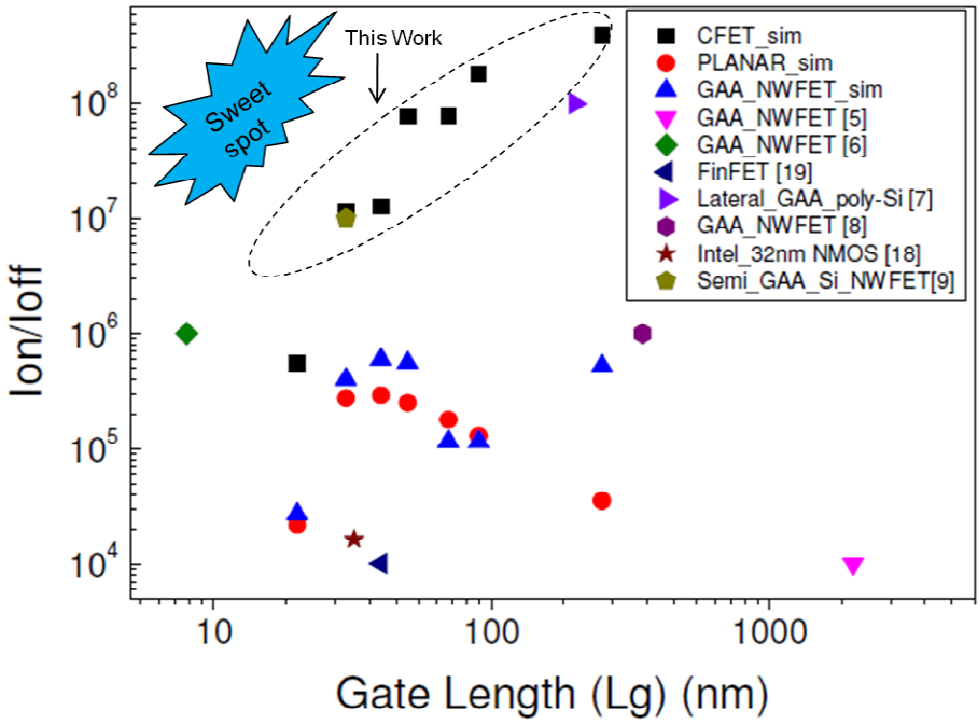

Fig. 2.7 Comparison of I_{on}/I_{off} performance of planar NMOS, GAA NWFET, CFET and current device demonstrations.

Other measures for characterizing a device`s performance is through the SS and the SCE. The SCE is a characteristic of short channel devices. The remainder of this chapter deals with the SCE of the CFET.

SS (Sub-Threshold Slope)

The sub-threshold slope of a device is obtained from the inverse slope of its Id-Vg plot in the linear region. It is usually a measure of how easily a device switches between its on (Idsat) and off (Ioff) states. Mathematically, the SS for a long-channel device is given by [15]:

$$SS = \left(\frac{d(log_{10}I_{ds})}{dV_{gs}}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right)$$

From to the above equation, the SS has a theoretical lower limit of 60 mV/dec, at room temperature. Therefore, it is desirable to have an SS value as close as possible to this theoretical limit. For conventional CMOS, the SS increases with aggressive scaling. Because of this, the SS for a short channel device has a modified equation given by [15]:

$$SS = 2.3\frac{kT}{q}\left(\frac{1}{\lambda} + \frac{C_{dm}}{C_{ox}}\right)$$

Here, λ is a factor that includes the effects of reducing the channel length. Although the CFET is not a planar SOI DGFET, it would be appropriate to include the modified expression for such a device for analytical purposes [15]:

$$SS = 2.3\frac{kT}{q}\left(\frac{1}{\lambda}\right)$$

On evaluating the above two expressions analytically, it can be seen that DGFETs tend to have a much lower sub-threshold slope compared to short – channel planar devices. Fig. 2.8 compares the simulated SS trend of the CFET with the simulated NMOS and GAA NWFET.

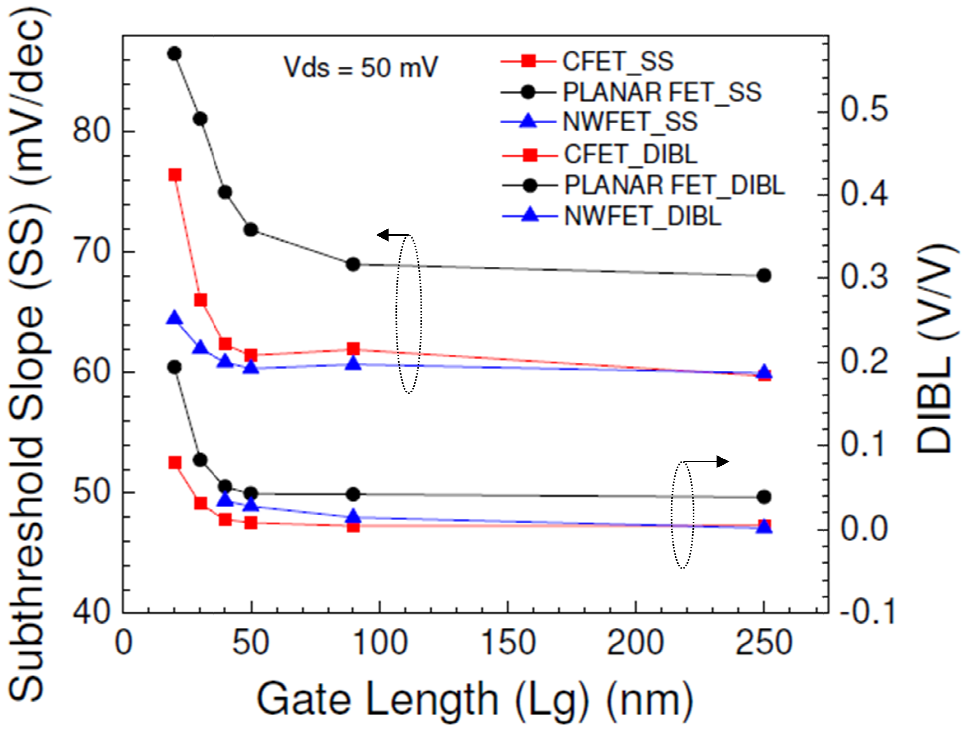

Fig. 2.8 SS and DIBL vs. gate length: Comparison between CFET, planar NMOS and GAA NWFET.

As it can be seen above, the SS of the CFET increases with decreasing gate length just like the NMOS. But unlike its conventional counterpart, the CFET has a very low sub-threshold slope, with the smallest device having an SS ~ 76 mV/dec. An interesting thing to note is that, the gate-all-around NWFET has the lowest and flattest SS trend.

V_t (Threshold Voltage) Roll-off

Due to aggressive scaling of CMOS devices, V_t - roll off has become an extremely important issue. This is a short channel effect (SCE) occurring due to a number of process related tolerances and can affect individual devices as well as whole wafers and lots. Channel length variation under high drain bias (Vds = Vdd) is one of the main

contributors to V_t roll off. Processes such as LDD (lightly doped drain) and Halo can cause these variations in channel length. As stated earlier current generation of CMOS devices are at the 32 nm technology node. This roughly translates to a gate length of 28 nm. At such dimensions, small gate length variations become significant enough to reduce the threshold voltage. Consequently, off current and sub-threshold slope are also affected. Fig. 2.9 shows how the threshold voltage of the CFET scales with the gate length.

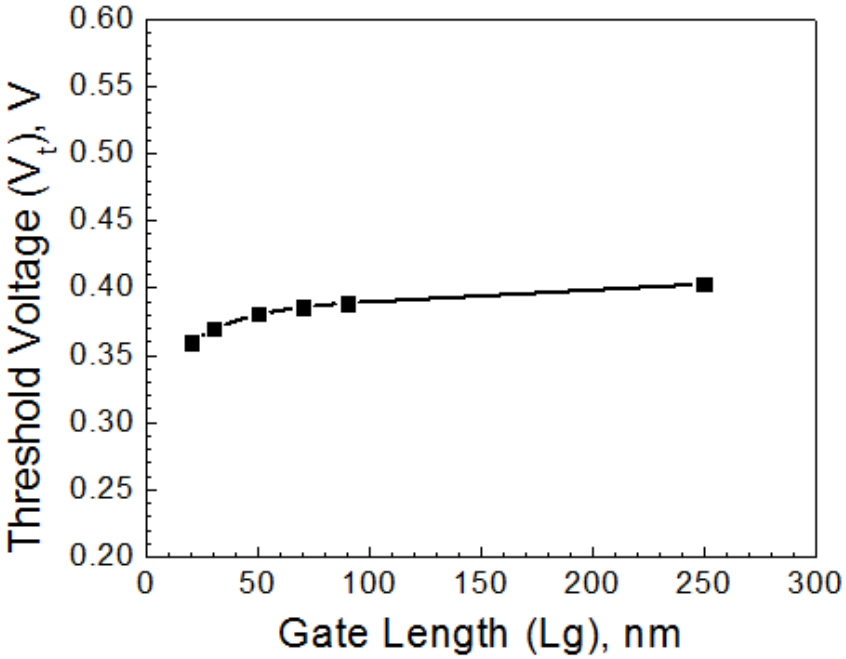

Fig. 2.9 CFET threshold votlage (Vt) variation with gate length (Lg).

The simulated CFET results indicate some roll off in the threshold voltage with decreasing gate lengths. However, this is very small and is confined between approximately 0.35 V and 0.4 V. Besides process related factors, V_t also depends on the materials used for the gate stack.

Another equally important contributor to SCE is random dopant fluctuations (RDF) in the channel region. Current CMOS devices require doping the channel in order to achieve the required threshold voltage. However, like in the previous case this is also process related. Recent simulation based studies have indicated that due to such fluctuations as well as positions of the dopants along the channel region can induce both positive and negative shifts in the threshold voltage [16][17].

DIBL (Drain – Induced Barrier Lowering)

Another measure to quantify the short channel effect (SCE) is the DIBL. For a planar NMOS, this can be understood by considering the potential barrier to electrons (p-type region in the NMOS). In the long channel case, biasing the device lowers this barrier and allows electrons to flow from the source to the drain. For the most part this barrier tends to remain flat under bias. However, in the short channel case, the potential barrier shrinks but is no longer flat. The point of maximum potential barrier (which lies at the center of the channel region) now starts shifting towards the source end. This continues until a bias point when the potential barrier just rolls off from the source to the drain and the gate loses control of the device. This shift in the maximum of barrier potential is called drain induced barrier lowering or DIBL. This explains the reduction in threshold voltage in short channel devices. Mathematically, The DIBL value is usually extracted from the linear and saturation Id-Vg curves using the following equation:

$$DIBL = \frac{|V_{tSat} - V_{tLin}|}{Vd_{Sat} - Vd_{Lin}}$$

Here, V_{tSat}, V_{tLin}, V_{dSat}, V_{dLin} are the threshold and drain voltages of the saturated and linear curves. In Fig. 2.8, the DIBL in the CFET is compared with that of the simulated NMOS and GAA NWFET. The 30 nm gate length CFET has a **DIBL** of **30.5 mV/V** for a V_{dSat} and V_{dLin} of 1V and 50 mV respectively.

Chapter 3: CFET – Device Fabrication Process Flow

One of the major plus points of the CFET is cost-effectiveness. Its unique architecture can be fabricated by an innovative process that is compatible with current CMOS technologies. Because it utilizes bulk silicon, it is a cheaper alternative to SOI based DGFETs, FinFETs and NWFETs. In addition to this, due to the epitaxial growth process, the CFET scaling is much easier since the gate length is defined by deposition rather than lithography. So scaling down to sub 10 nm gate lengths is possible without resorting to extreme lithography. In order to fabricate the cylindrical field effect transistor the following process flow is proposed. The layer thicknesses used in the flow correspond to a CFET with ring width 20 nm and 30 nm channel length. The layers are not drawn to scale.

1. A P+ <100> oriented silicon wafer is used as the substrate. 40 nm of nitride is deposited on the wafer. Next 30 nm of TiN is deposited and on top of this 40 nm of isolation oxide is deposited. The TiN metal serves as the gate material for the CFET.

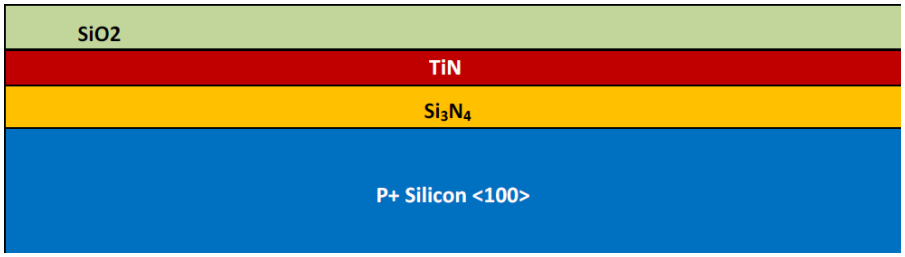

Fig. 3.1 Stack Deposition

2. To define the cylindrical structure of the CFET, the dark field mask (Fig. 3.2) is used for patterning the gate stack. The ring width of the mask circle is relaxed and can be as large as 100 nm. This nearly vertical trench etch of a multi-material stack has already been successfully demonstrated in the Integrated Nanotechnology Fab group at KAUST (shown at the end of the process flow in Fig. 3.11).

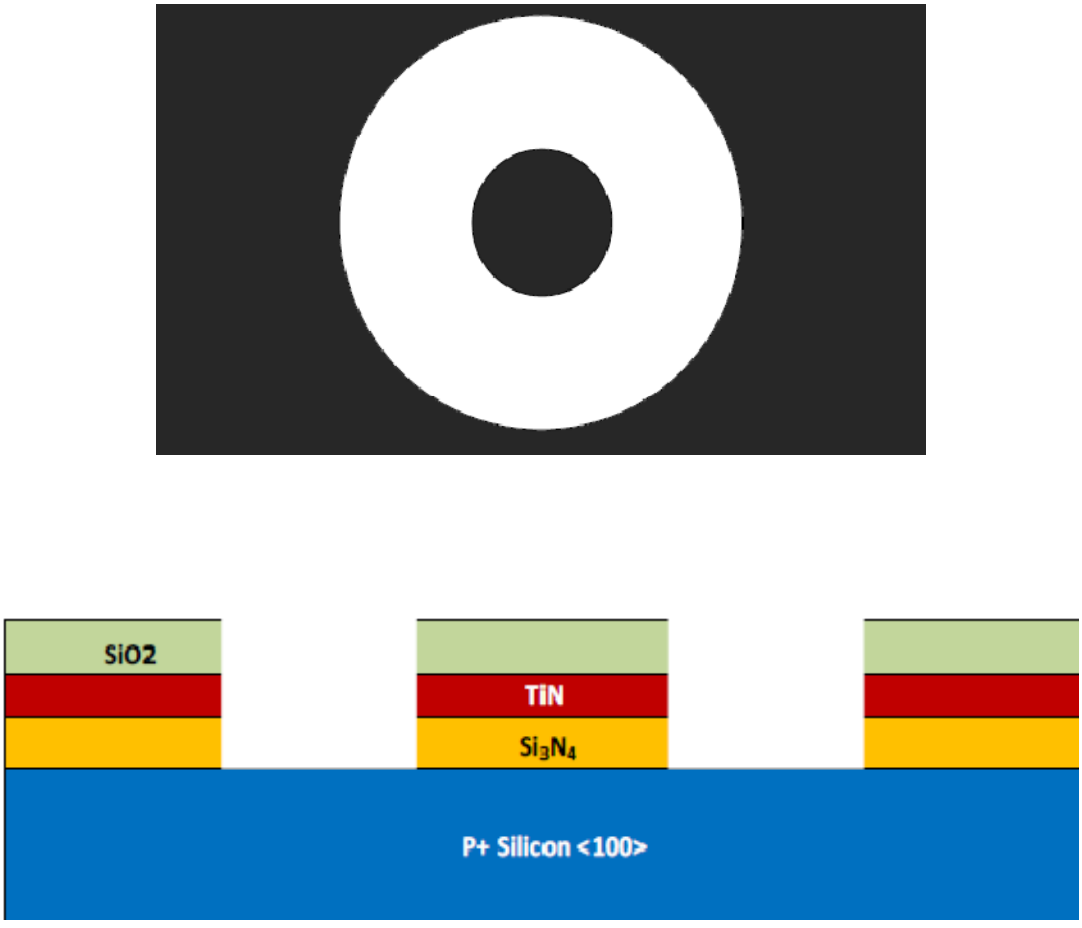

Fig. 3.2 (Top) Mask with 100 nm opening. (Bottom) Trench etch of material stack after pattering.

3. If the mask has a ring width of 100 nm, then a 40 nm thick nitride spacer is deposited after the trench etch as indicated below.

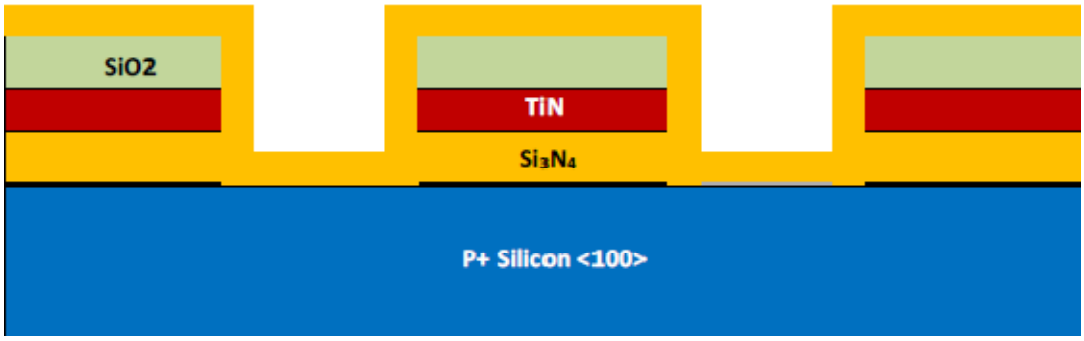

Fig. 3.3 Nitride Spacer Deposition

4. A highly anisotropic etch is carried out next. This etch removes all of the unprotected nitride on the horizontal surfaces leaving behind vertical sidewall spacers. After this etch step, each opening (from the previous trench etch) has got two 40 nm sidewall spacers. This leaves 20 nm openings which sets up the final ring width of the device.

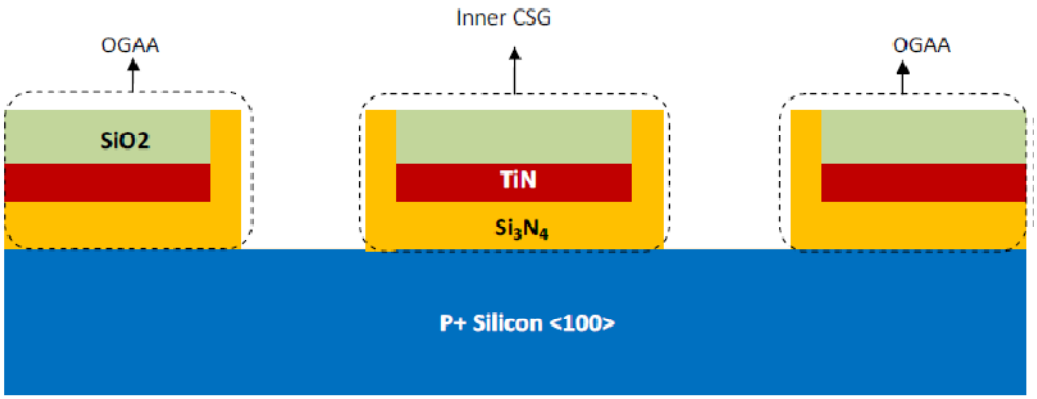

Fig. 3.4 Anisotropic Nitride Etch

5. The next step involves formation of the source region. A low energy heavy dose of Arsenic is ion implanted to form the heavily doped (n++) source as shown below:

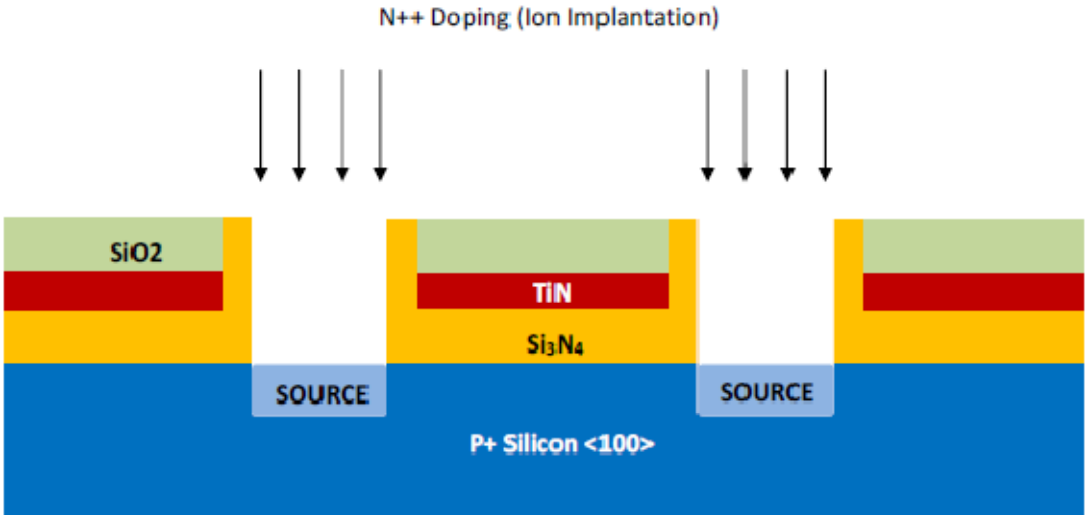

Fig. 3.5 Source Formation.

6. After the source definition, epitaxial silicon is grown from the openings. Epi silicon is allowed to grow till it ‘mushrooms’ over the gate stack as shown below. The ‘mushroomed’ portion will serve as the CFET drain. As the pristine epitaxial silicon is free from any doping, there are minimal random dopant fluctuations (RDF) as described in chapter 2.

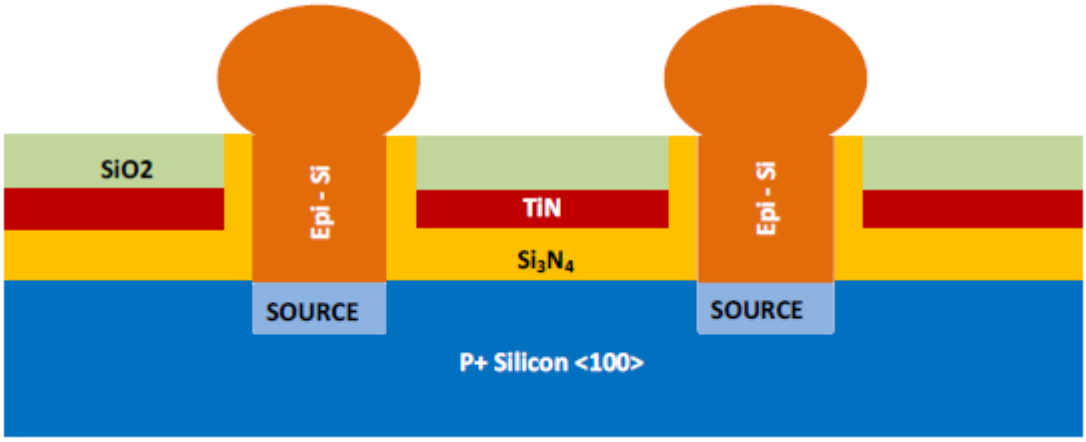

Fig. 3.6 Channel/Drain growth by Epitaxy.

7. The next step involves formation of the CFET drain. Just like for the source region, a heavy dose of Arsenic is implanted at a low energy in the mushroomed epitaxial silicon. After this is done, a flash anneal step may be performed for dopant activation in the source and drain.

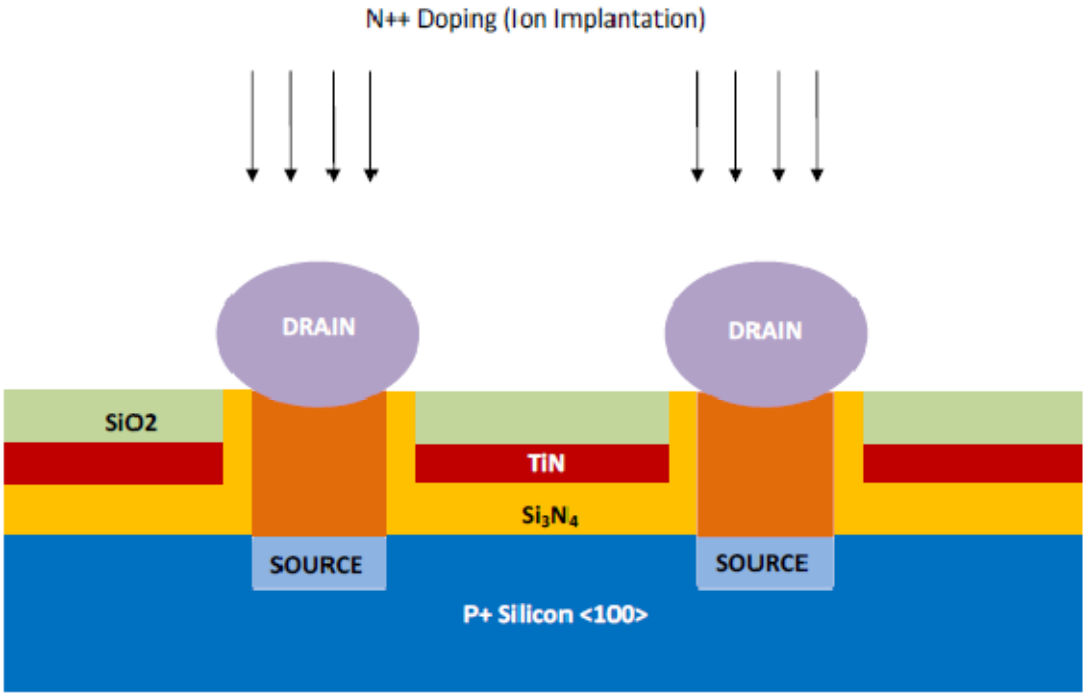

Fig. 3.7 Drain Formation.

8. After the formation of the gate, drain and source, a thick Inter Layer Dielectric (ILD) is blanket deposition. This step is required for contact definition.

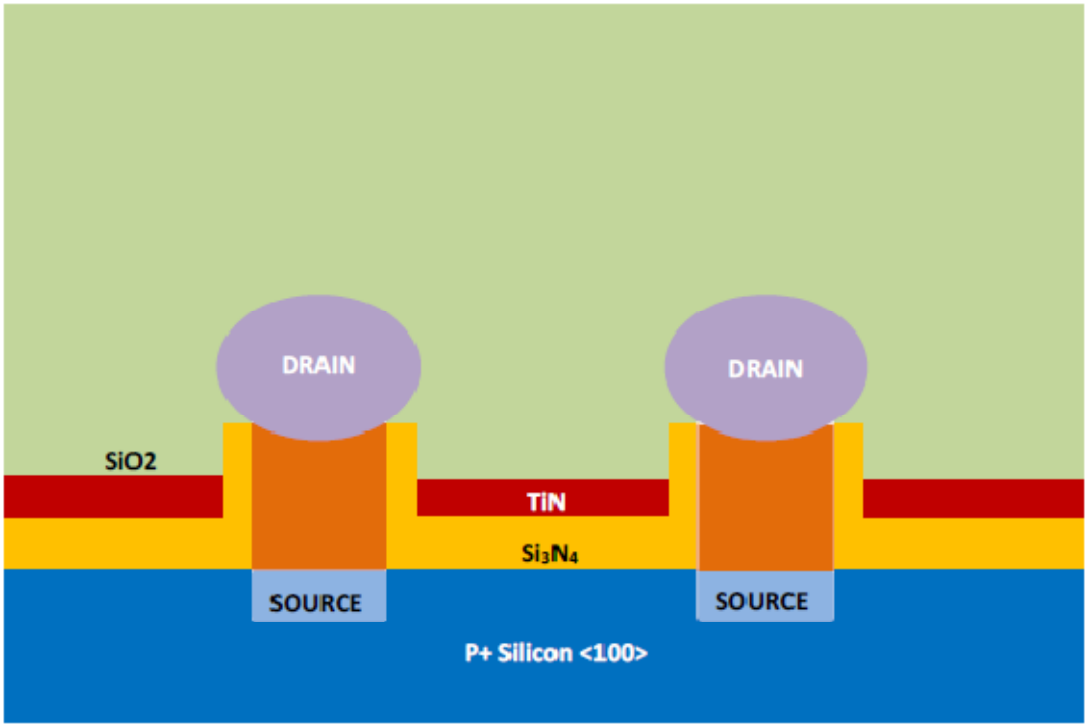

Fig. 3.8 Deposition of Interlayer Dielectric Material.

9. Contact holes are then etched through the ILD layer to create openings to the inner core shell gate (CSG), the outer gate (OGAA) and the drain. No contact holes need to be defined for the source. A back contact to the initial support wafer is used for source biasing.

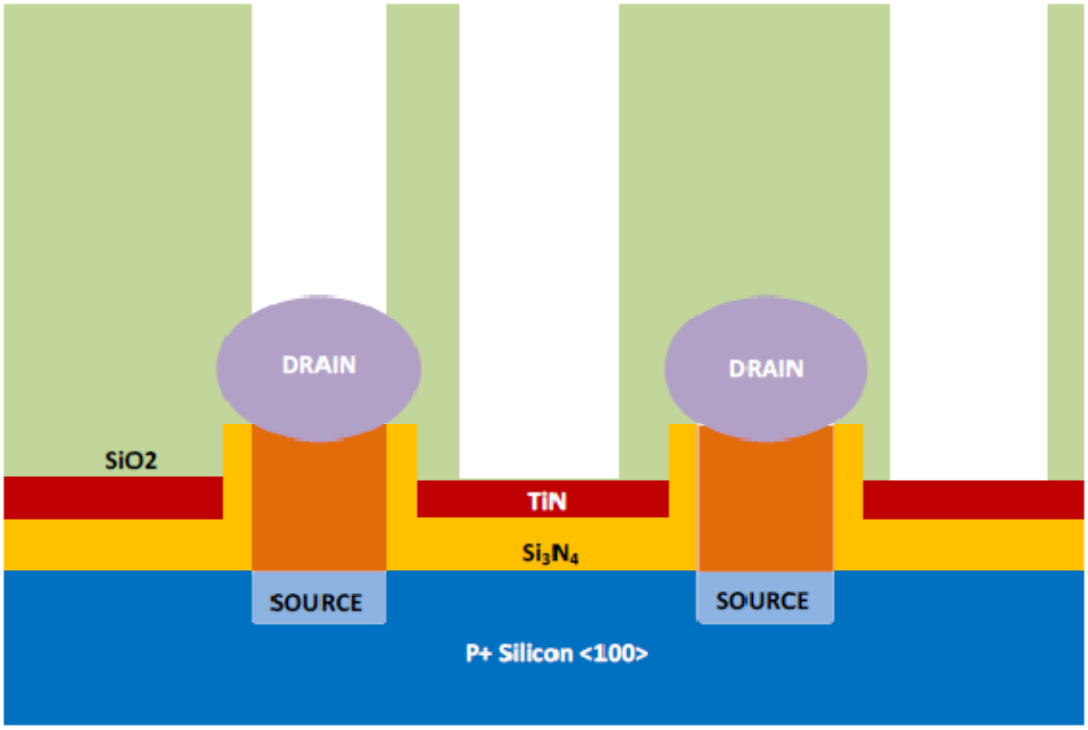

Fig. 3.9 Contact hole etching.

10. Finally, the etch holes are filled with a bulk contact material such as tungsten. The 2D cross-section shows the final device structure of the CFET with all the contact placements.

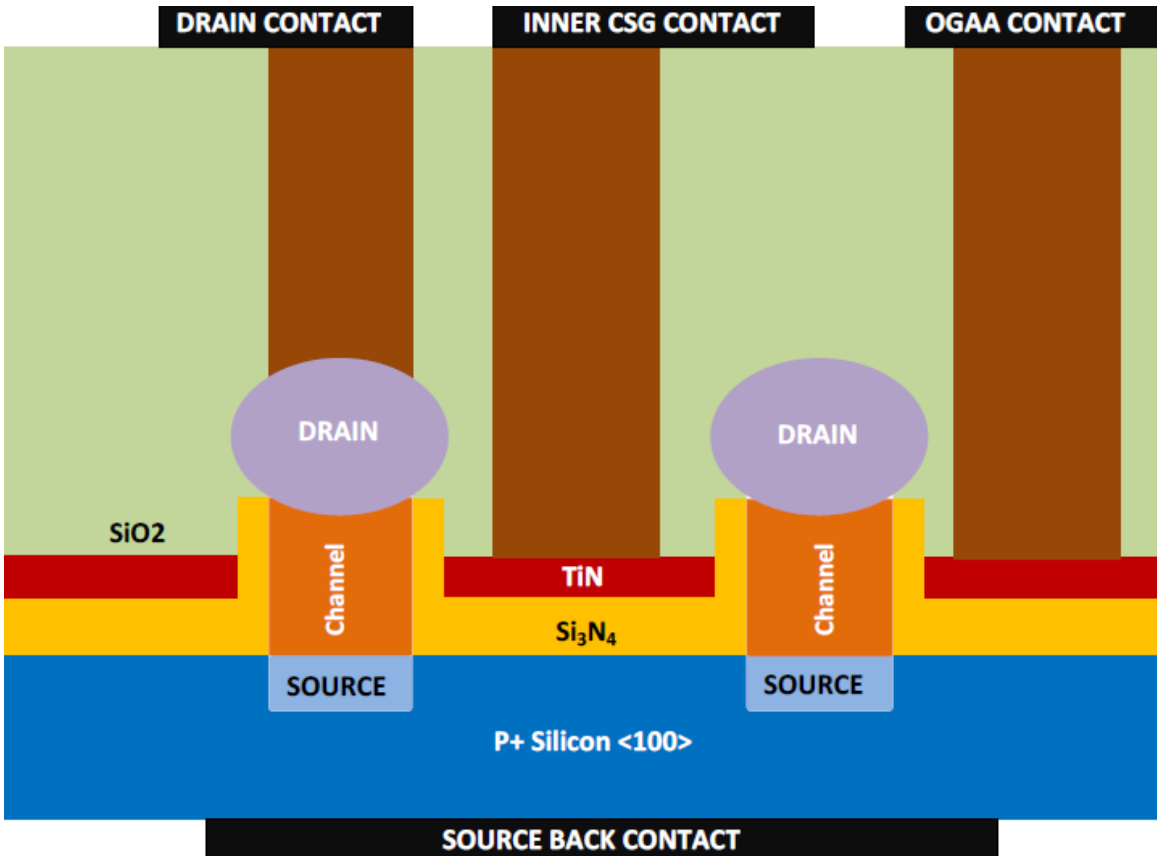

Fig. 3.10 Contact etch hole fill and contact placement.

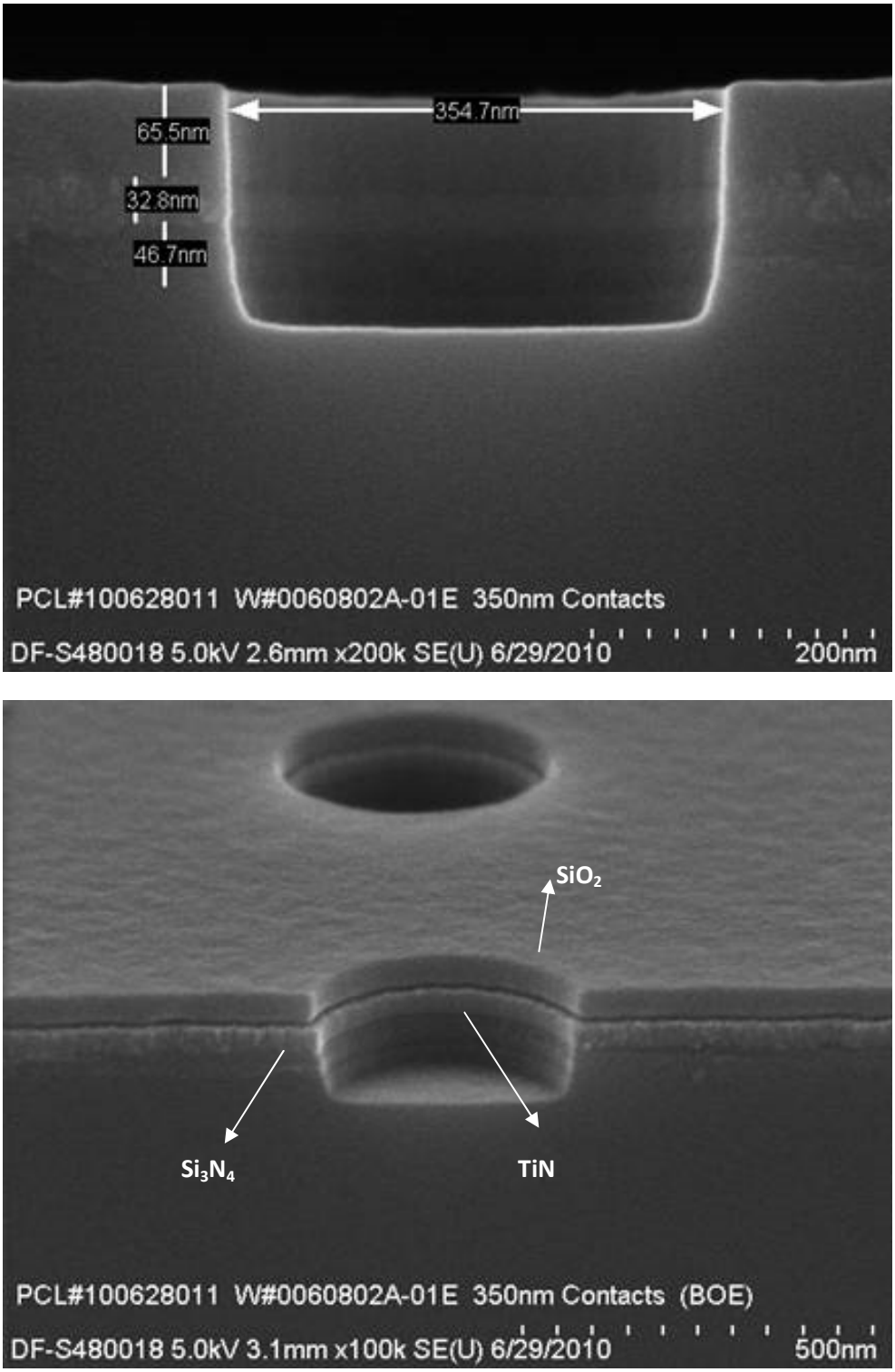

Fig. 3.11 (Top) SEM of SiO2/TiN/Si3N4 stack after vertical trench etch. (Bottom) Tilted view of the stack.

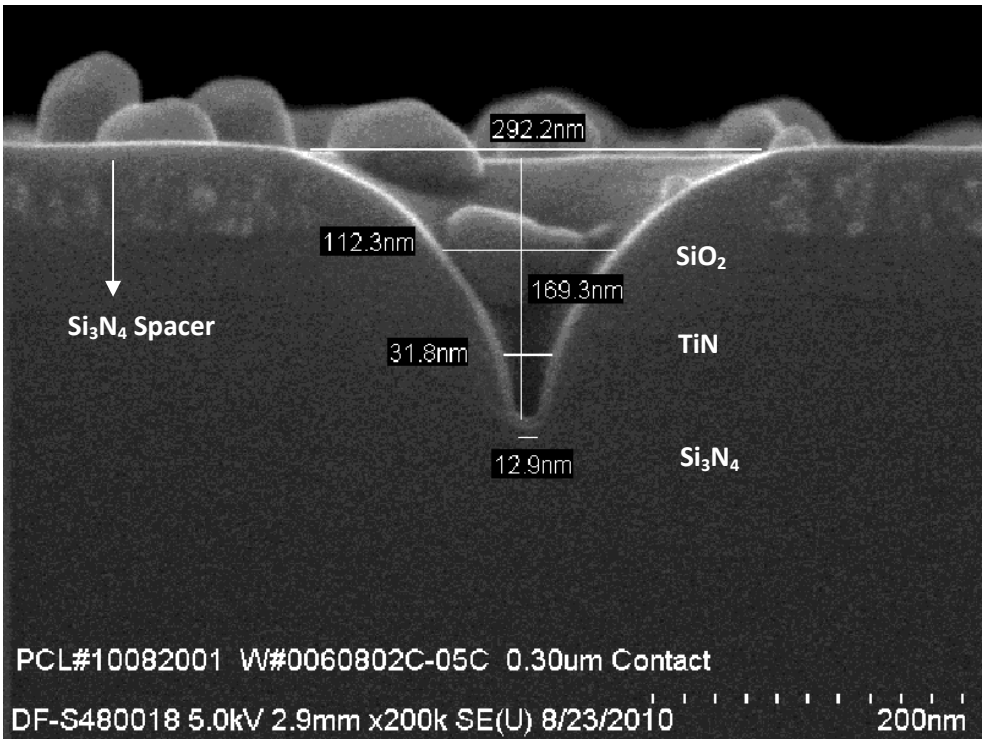

Fig. 3.12 SEM of SiO2/TiN/Si3N4 stack after Nitride spacer deposition

Conclusion

To conclude this thesis, a summary of the accomplishments is provided in this section. This thesis started off with an insight into the current state of CMOS devices. In order to continue the scaling trend, the need for new and innovative device architectures has been emphasized. A brief walkthrough on the evolution of DGFETs, FinFETs and NWFETs was provided. Based on this, the unique CFET device was proposed. Chapter 1 discussed the architecture of the CFET device. In order to test the feasibility of such a device, TCAD simulations were carried out as shown in chapter 2. Device operation based on volume inversion and performance enhancements as well as comparison against other novel and bulk CMOS devices was done. In chapter 3, a simple CMOS compatible fabrication flow was proposed for the CFET. In summary, the following has been the highlights of this thesis:

- Volume inversion in the CFET can be attained with a thick silicon body unlike other devices such as the DGFET and the NWFET [22][23]. Results indicated that volume inversion can be obtained in the CFET with silicon bodies up to 40 nm thickness.
- High drive current and enhanced I_{on}/I_{off} ratio has been shown in the CFET as opposed to other device types [22][23]. Simulation results attributed this to increased carrier concentrations and near- ballistic carrier velocities in the device channel.

- Simulations also showed excellent electrostatic control in the CFET channel through near ideal sub-threshold slopes and low drain induced barrier lowering. In addition to this, the short channel effect was reduced in the CFET. This is indicated by a small V_t roll off with gate length reduction. Use of un-doped epitaxial silicon channel was used to mitigate random dopant fluctuations (responsible for inducing threshold voltage shifts).

Besides the above obvious advantages, the CFET can provide a cost effective alternative to DGFETs, NWFETs and FinFETs as discussed in chapter 3. Sub-10 nm gate length CFETs are easy to fabricate as opposed to other device architectures. Unlike conventional CMOS, DGFETs, NWFETs, the gate length is defined by a deposition controlled growth. All of this favors the CFET as a superior alternative to future replacement devices such as DGFETs, FinFETs and NWFETs.

Future Research Objectives

The next objective of the CFET project is validation of simulation results. This entails device fabrication and demonstration. Improving device performance forms the basis for further exploratory work. This involves experimentation with alternate epitaxially grown III-V channel materials. In addition to this, p-channel CFET simulation and fabrication is an added incentive for further research in this project.

Bibliography

[1] International Technology Roadmap for semiconductors, 2009.

[2] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa, "Double-Gate Silicon-on-Insulator Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance", pp. 410-413, 1987, Vol. EDL-8, No. 9, *IEEE Electron Device Letters.*

[3] D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda,"A Fully Depleted Lean-Channel Transistor (DELTA) – A Novel Vertical Ultrathin SOI MOSFET", pp. 36-39, Jan. 1990, Vol. 11, No. 1, *IEEE Electron Device Letters.*

[4] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.J. King,, J. Bokor and C. Hu, "FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20nm", pp. 2320-2326, Dec. 2000, Vol. 47, No. 12, *IEEE Trans. on Electron Devices.*

[5] G. Zheng, W. Ly, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," pp. 1890–1893, vol. 16, no. 21, Nov. 2004, *Adv. Mater.*

[6] Y. Jiang, T. Y. Liow, N. Singh, L. H. Tan, G. Q. Lo, D. S. H. Chan and D. L. Kwong, "Performance Breakthrough in 8nm Gate Length Gate-All-Around Nanowire Transistors using Metallic Nanowire Contacts," pp. 34-35, 2008, *IEEE Symp. on VLSI Tech. Dig.*

[7] P. Kalavade and K. C. Saraswat, "Lateral Gate-All-Around (GAA) poly-Si transistors," pp. 109-110, 2001, *IEEE International SOI Conf.*

[8] N. Singh et al., "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance," pp. 1-4, 2006, *IEDM.*

[9] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada, H. Iwai, "High-performance Si Nanowire FET with a semi gate-around structure suitable for integration," pp. 249-252, 2009, *ESSDERC proceedings.*

[10] J. R. Heath, "Superlattice Nanowire Pattern Transfer (SNAP) ," Jan. 2008, *Accounts Of Chemical Research.*

[11] K. Blotekjaer, "Transport Equations for Electrons in Two-Valley Semiconductors," pp. 38-47, Vol. ED-17, No. 1, 1970, IEEE *Trans. on Electron Devices.*

[12] R. Stratton, "Diffusion of Hot and Cold Electrons in Semiconductor Barriers," pp. 2002-2014, Vol. 126, No. 6, 1962, *Physical Review.*

[13] F. Gamiz, M.V. Fischetti, "Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion," pp. 5478-5487, Vol. 89, No. 10, May 2001, *J. of App. Phys.*

[14] Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI devices," pp. 192-195, 2nd Edition, 2009.

[15] A. Godoy, J.A. Lopez-Villanueva, J.A. Jimenez-Tejada, A. Palma and F. Gamiz, "A simple subthreshold swing model for short channel MOSFETs," pp. 391-397, 45, Jan. 2001, *Solid-State Electronics.*

[16] A. Asenov, "Random Dopant IInduced Threshold Voltage Lowering and Fluctuations in Sub-0.1 m MOSFET's: A 3-D "Atomistic" Simulation Study," pp. 2505-2513, Vol. 45, No. 12, Dec. 1998, *IEEE Transc. On Electron Devices.*

[17] R. Rao, N. DasGupta, A. DasGupta, "Study of Random Dopant Fluctuation Effects in FD-SOI MOSFET Using Analytical Threshold Voltage Model," pp. 247-253, Vol. 10, No. 2, June 2010, *IEEE Transc. On Device and Materials Reliability.*

[18] P. Packan, S. Akbar, M. Armstrong, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golozonka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, A. St. Amour, K. Kone, T. Troeger, C. Weber, K. Zhang, S. Natarajan,"High Performance 32nm Logic Technology Featuring 2nd Generation High-K + Metal Gate Transistors," pp. 28.4.1-28.4.4, 2009, *IEDM.*

[19] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick and R. Chau, "Tri-gate Transistor Architecture with High-K Gate Dielectrics, Metal Gates and Strain Engineering," 2006, *IEEE Symp. on VLSI Tech. Dig.*

[20] M. Lundstrom, Z. Ren, "Essential Physics of Carrier Transport in Naanoscale MOSFETs," pp. 133-142, Vol. 49, No. 1, Jan. 2002, *IEEE Transc. On Electron Devices.*

[21] Available: Sentaurus Device Manual.

[22] K. Uchida, J. Koga, S. Takagi, "Experimental Study on Carrier Transport Mechanisms in Double- and Single-Gate Ultrathin-Body MOSFETs – Coulomb

Scattering, Volume Inversion, and δT_{SOI}-induced Scattering," pp. 33.5.1-33.5.4, 2003, *IEDM.*

[23] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Rustagi, G. Q. Lo, N. Balasubramanium, and D. L. Kwong, "Si, SiGe Nanowire Devices by Top-Down Technology and Their Applications," pp. 3107-3119, Vol. 55, No. 11, Nov. 2008, *IEEE Trans. on Electron Devices.*

[24] D.W.Wang, Q.Wang, A. Javey, R. Tu, H. J. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, "Germanium nanowire field effect transistors with SiO2 and high-κ HfO2 gate dielectrics," pp. 2432–2434, Vol. 83, No. 12, , Sep. 2003. *Appl. Phys. Lett.*

[25] L. Zhang, R. Tu, and H. Dai, "Parallel core-shell metal–dielectric–semiconductor germanium nanowires for high-current surround-gate field-effect transistors," pp. 2785–2789, Vol. 6, No. 12, Oct. 2006, *Nano Lett.*

[26] S. A. Dayeh, D. P. R. Aplin, X. T. Zhou, P. K. L. Yu, E. T. Yu, and D. L. Wang, "High electron mobility InAs nanowire field-effect transistors," pp. 326–332, Vol. 3, No. 2, 2007, *Small.*

[27] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan and C. M. Leiber, "Ge/Si nanowire heterostructures as high-performance field effect transistors," 441, 481-493, 2005, *Nature.*